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| 09/752,594 | 12/27/2000 | Terry L. Kendall | 42390P10071 | 1642 |
| 7590 06/01/2004 | | | EXAMINER | |
| George B. Leavell | | | GOSSAGE, GLENN A | |
| BLAKELY, SO | KOLOFF, TAYLOR & 2 | ZAFMAN LLP | | |
| Seventh Floor | | | ART UNIT | PAPER NUMBER |
| 12400 Wilshire | | | 2187 | 10 |
| Los Angeles, CA 90025-1026 | | | DATE MAILED: 06/01/2004 | |

Please find below and/or attached an Office communication concerning this application or proceeding.

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|--|---|---|----------|--|--|--|
| | Application No. | Applicant(s) | m | | | |
| • | 09/752,594 | KENDALL ET AL. | • | | | |
| Office Action Summary | Examiner | Art Unit | | | | |
| | Glenn Gossage | 2187 | | | | |
| - The MAILING DATE of this communication app | <u> </u> | ith the correspondence address - | - | | | |
| Period for Reply | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the malling date of this communication. If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply specified above, the maximum statutory period of Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). | 38(a). In no event, however, may a y within the statutory minimum of thir will apply and will expire SIX (6) MOR , cause the application to become A | reply be timely filed ty (30) days will be considered timely. ITHS from the mailing date of this communication BANDONED (35 U.S.C. § 133). | aton. | | | |
| Status | | | | | | |
| 1) Responsive to communication(s) filed on 10 M | lay 2004. | | | | | |
| 2a) ☐ This action is FINAL . 2b) ☑ This | action is non-final. | | | | | |
| 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is | | | | | | |
| closed in accordance with the practice under E | Ex parte Quayle, 1935 C.E | D. 11, 453 O.G. 213. | | | | |
| Disposition of Claims | | | | | | |
| 4)⊠ Claim(s) <u>1-14 and 17-24</u> is/are pending in the | application. | | | | | |
| 4a) Of the above claim(s) is/are withdraw | wn from consideration. | | | | | |
| 5) Claim(s) is/are allowed. | | | | | | |
| 6) Claim(s) <u>1-14 and 17-24</u> is/are rejected. | | • | | | | |
| 7) Claim(s) is/are objected to. | | | | | | |
| 8) Claim(s) are subject to restriction and/o | r election requirement. | | | | | |
| Application Papers | | | | | | |
| 9)⊠ The specification is objected to by the Examine | er. | | | | | |
| 10) The drawing(s) filed on is/are: a) acc | epted or b) objected to | by the Examiner. | | | | |
| Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | |
| Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). | | | | | | |
| 11) The oath or declaration is objected to by the Ex | xaminer. Note the attache | d Office Action or form PTO-152 | <u> </u> | | | |
| Priority under 35 U.S.C. § 119 | • | | | | | |
| 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: | priority under 35 U.S.C. | § 119(a)-(d) or (f). | | | | |
| Certified copies of the priority documents have been received. | | | | | | |
| 2. Certified copies of the priority documents have been received in Application No | | | | | | |
| 3. Copies of the certified copies of the priority documents have been received in this National Stage | | | | | | |
| application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| See the attached detailed Office action for a list | of the certified copies no | received. | | | | |
| Attachment(s) | _ | | | | | |
| Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) | | Summary (PTO-413) (s)/Mail Date | | | | |
| Notice of Dratisperson's Patent Drawing Review (FTC-946) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date | | Informal Patent Application (PTO-152) | | | | |

U.S. Patent and Trademark Office PTOL-326 (Rev. 1-04)

Office Action Summary

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1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 6, 2003 have been approved by the Examiner, subject to drafting review. Corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "circuit to send," which is within the host processor, and "circuit to exit," of claim 13; the "circuit to verify," within the host processor, of claim 14; and the "circuitry to determine" (within the "circuit to verify"?) of claim 17; the "circuit to reprogram" of claim 18; and the "circuit one word that did not verify" (?) of claim 19, must be shown or the features canceled from the claims. No new matter should be entered.

In this regard, applicants' arguments filed October 6, 2003 have been considered but are not persuasive.

The reference to page 10 of the specification is not entirely understood since the cited passage does not appear to describe a "circuit to exit," "circuit to reprogram," etc. Moreover, while the processor or "processing circuitry" is shown, the individual circuits <u>as claimed</u> are not shown as required by 37 CFR 1.83(a). Since applicants choose to claim the individual circuits (as opposed to the host processor or processing circuitry performing the functions, e.g.), the individual circuits must be shown.

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3. It is once again noted that the disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 3, line 21, it appears "program" should be --programming-- for clarity and consistency (see line 16, e.g.).

On page 11, line 21, it appears "a" (second occurrence) should be deleted for clarity.

On page 12, line 21, it appears --flash memory-- should be inserted before "device" for consistency (note lines 14 and 16, e.g.).

On page 16, lines 17 and 19, it appears "117a-117p" should be --117A-117P-- for consistency (with Figure 6). See also page 29, lines 5, 7, 8 and 10.

On page 37, line 13, it appears --or procedures-- should be inserted before "320" for consistency (see line 9, e.g.), since the use of different names (operations, flow, procedures, technique) for the same reference numeral (320) is confusing. Similarly, it appears --for procedure-- should be inserted before "320" in line 17 for consistency (again see line 9, e.g.). See also page 39, lines 12 and 17; page 40, line 18; and page 41, lines 4 and 10, which should also be amended to use consistent terminology.

On page 40, in the first paragraph as amended in the response filed October 6, 2003, at line 12 of the paragraph, it appears "compare" should be changed to --be the same-- for clarity and consistency (note lines 7-8 of the paragraph, e.g.). Similarly, in line 14 of the paragraph, it

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appears "substantially" should be deleted for clarity and consistency (to avoid possible questions of new matter). Again see lines 7-8 of the paragraph.

On page 43, line 2, it appears --or lines-- should be inserted before "26" for consistency (see page 10, line 2, e.g.).

Again note that these are merely exemplary. The entire specification should be <u>carefully</u> and <u>completely</u> reviewed to ensure that all possible errors are located and corrected. Note that many of these issues/objections were not addressed, by way of either amendment or argument, in the response filed October 6, 2003.

In the claims:

In claim 1, line 4, it appears "the" should be deleted for clarity.

In claim 2, line 3, "the" (second occurrence) appears to read more clearly here as --a--.

In claim 5, line 5, it appears --internal program-- should be inserted before "verification" for clarity and consistency (see claim 1, line 7, e.g.). See also claim 6, line 5.

In claim 8, line 2, it appears "the" should be deleted for clarity.

In claim 9, line 1, it appears --the-- should be inserted before "programming" for clarity and consistency (note claim 10, line 1, e.g.).

In claim 19, line 3, it appears "are not verified" should be changed to --did not verify-- for clarity and consistency with the originally filed disclosure (note original claim 19, e.g.).

Appropriate correction is required.

4. Claims 13-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, and therefore its dependent claims, the relationship between the "automation circuitry" and the "special programming circuitry" is not adequately clear. [Should "disabled; a" in lines 4-5 be changed to --disabled, said automation circuitry including--, for clarity? Note Figures 4 and 5.]

Also, it is not sufficiently clear to what the "circuitry to send" and "circuit to exit," which are within the "host processor," refer here, or how they are connected or related to the other elements set forth in the claim.

Applicants are again respectfully reminded that while 35 U.S.C. 112 sixth paragraph permits the use of functional language in a claim, this provision must always be considered as subordinate to the second paragraph of 35 U.S.C. 112 (see *In re Lundberg*, 244 F.2d at 547-548, 113 USPQ at 534 (CCPA 1979)). If one employs functional language in a claim, one must set forth an adequate disclosure showing what is meant by that language. If applicant fails to set forth such an adequate disclosure, applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112. See *In re Donaldson Company, Inc.*, 29 USPQ 2nd 1845 (Fed. Cir. 1994).

In the instant case, the language of the specification and claims is such that applicant has failed to provide an adequate disclosure showing to what the "circuitry to send" and "circuitry to exit" refer in this instance. The terms and phrases used in the claims must find clear support or

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antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (in this regard, see also 37 CFR 1.75(d)(1)).

In claim 14, it is not sufficiently clear to what the "circuitry to verify" within the "host processor" refers here. [Should "further includes a circuit to verify" in lines 1-2 be changed to simply --verifies--?]

In claim 15, it is not clear to how the host processor "includes" a verification processor (support for language in the specification?). [Should "host processor" in line 1 be changed to -- circuit to verify--? Note original claim 14. simply --verifies--?]

In claim 16, it is not clear how the memory itself includes the verification processor (note claim 15, e.g.).

In claim 17, it is not sufficiently clear to what the "circuitry to determine" refers here, or how it is connected or related to the other elements in the claims. It is also not sufficiently clear to what the "circuitry to comparing" refers here, or how it is connected or related to the other elements in the claims. The proper antecedent for "the memory" in lines 6-7 is also not entirely clear since there are two memories set forth in the claims.

In claims 18 and 19, it is not clear to what the "circuit to reprogram" refers here, or how it is connected or related to the other elements in the claims. [Should "further comprises a circuit to reprogram" in lines 1-3 be changed to simply --reprograms--?]

In this regard, applicant's arguments filed October 6, 2003 have been considered but are not persuasive. With respect to the various claimed "circuits," attention is respectfully directed to the comments in numbered paragraph 2 above. Again, if applicants choose to claim the

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individual circuits, it should be clear from reading the specification and/or drawings disclosure to what the claimed circuits refer, so that one may ascertain what equivalents there might be to these circuits. In the instant case, since one is unable to ascertain, with a reasonable degree of certainty, to what the claimed circuits refer when reading the disclosure, applicants have failed to particularly point out and distinctly claim the subject matter of the invention.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 09/748,825. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims

a method and apparatus for programming a memory, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a

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plurality of words into the memory without the memory performing internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to enabling internal program verification with the consequent loss of their function, would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made, anticipation being the epitome of obviousness. See particularly claims 1-2, 15-16 and 22-23, for example. Note also that the commonly assigned patent also claims subsequently enabling internal program verification, as well as having a host processor verify external to the memory the programming of the plurality of data words into the memory. The commonly assigned patent also claims disabling entry into the special program mode of the memory, as well as using only a single programming pulse for each bit of each word of the plurality of words, and sending a data word to the memory for reprogramming.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1-24 are also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/749,133. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for performing programming operations in a memory as in the present invention, the method including entering a special programming mode of a memory that

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disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to hashing words and comparing hash values, with the consequent loss of their function, would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made. See particularly claims 1, 14 and 17, for example. The commonly assigned patent also claims enabling internal program verification, as well as programming a plurality of words, and using a host processor as a "verification processor" to verify the programming during a special programming mode.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Applicants' indication in the response filed October 6, 2003 that "a terminal disclaimer will be submitted upon the allowance or patenting with one or more claims" (response at page 18) is noted. It is also noted that at least one of the commonly assigned copending applications has been allowed.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al.

With respect to claim 1, as well as claim 13, a method for programming a memory including enabling a "special" or test programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification, was known in the art at the time the claimed invention was made. See, for example, Intel Corporation Application Note AP-629 or AP-678, each taken separately. As one of ordinary skill in the art would readily appreciate, a plurality of words may be programmed into the memory during a "special" or test mode, and the "special" or test programming mode exited after the tests are performed. The programming modes of a flash memory are controlled by a write state machine in a well known manner. The use of a write state machine allows the sequence of steps necessary to perform a programming operation to be easily controlled or automated. The various modes may be entered by entering a certain command or "code" in a command register which is forwarded to the write state machine. See, particularly, Figure 1 of Application Note AP-678

Application Note AP-629 also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (see AP-629, at page 9, as well as page 10 and Figure 4). Application

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Note AP-629 further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (see AP-629, at page 9, column 2, e.g.).

Application Note AP-678 similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2, e.g.).

The Application Notes only specifically discuss saving time by not performing program verify operations with the external ATE, and do not teach disabling internal program verification operations during the "special" programming mode so that a plurality of words are programmed in the "special" or test mode without the memory performing internal program verification.

Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines and 7-12 32-36, e.g.). Olivo teaches that overall testing speed may be improved, and that various testing values or parameters may be selected at will so that the memory test can be made fully independent of the control unit and the internal state machine (see column 5, lines 1-10, as well as column 1, lines 40-62, e.g.).

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Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to disable program verification operations by an internal state machine during a "special" programming mode, as taught by Olivo et al, in the flash memory apparatus and method of Intel Corporation Application Note AP-629 or AP-678, each taken separately, so that a plurality of words may be programmed without the memory performing internal program verification, because the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one should consider modifying the method or program flow to perform only necessary operations, and Olivo teaches that an improved testing speed and greater flexibility in the testing process may be obtained by disabling or not performing internal program verification operations. The improvement in testing speed and ability to change the testing process independent of the control unit and internal state machine as taught by Olivo et al provide ample motivation and suggestion to disable internal program verification operations in a memory such as in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, so as to avoid redundant program verify operations while providing an improved test speed and increased flexibility in the testing process.

With respect to claims 2-3 and 14-15, one of ordinary skill in the art would readily appreciate that the automated test equipment in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, may include processor and that the memory may be tested by resending a plurality of words previously sent into the memory (note page 3, lines 3-15 of the present specification, e.g.).

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With respect to claims 4-6 and 8, as well as claims 16-18 and 20, internal program verification by the memory may be enabled after the memory is tested so that the user can be assured that data is being properly programmed and is reliable. The programming and testing of nonvolatile memories is an iterative process so that if one of the plurality of words does not verify, the programming and verification are repeated (see page 2, lines 15-20 of the present specification, e.g.). If all of the plurality of words verify, the programming mode may be exited.

As per claims 7 and 19, one of ordinary skill in the art would recognize that the "special" programming mode may be permanently disabled after being tested at the factory so that a user is not able to enter the "special" programming mode.

With respect to claims 9 and 21, one of ordinary skill in the art would recognize that the number of iterations in the programming or testing sequence may obviously be varied. The ability to simply change the testing procedure is a key aspect of the teachings of Olivo et al, and the selection of a single iteration or a single programming pulse in order to quickly test the memory would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

With respect to claims 10-12 and 22-24, the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that programming the plurality of words into the memory may continue until a programming ending condition is met (see page 4, line 14 to page 5, line 3 of the present specification, e.g.). As one of ordinary skill in the art would readily appreciate, the programming ending condition may be that a pre-selected time has elapsed (a "timeout"

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condition has occurred) or an ending address (the last address in the memory has been reached and the entire memory has been tested).

7. Applicants' arguments filed October 6, 2003 have been considered but are not persuasive. It is believed applicants' arguments have been addressed in the preceding paragraphs.

Also, the argument that Olivo does not disclose or suggest disabling internal program verification operations during a "special" programming mode is not persuasive. The response argues that Olivo teaches that memory cells can be verified and that some verification is performed, referring to column 4, lines 32-36 and column 4, line 63 to column 5, line 10 (response at pages 21-22), and thus Olivo does not teach disabling the internal program verification operations. However, Olivo does teach disabling internal program verification operations during a "special" test mode while permitting some verification to be selectively performed just as in the claimed invention (see column 2, lines 13-16 and 28-31 and claim 10, step A of Olivo and also see pages 10 and 11, lines 17-18 and claims 14 and 15 of the present application, e.g.).

The argument that there is no motivation to combine the teachings of the references is also not persuasive. Olivo clearly teaches that by disabling an internal program verification operation, tests can be performed in a manner fully independent of control circuitry such as the internal write state machine and various parameters may be selected at will. The ability to independently perform verification or testing operations in a flash memory fully independent of the memory control circuitry provides ample motivation and suggestion to one of ordinary skill in the art to disable internal write state machine for controlling verification operations in the

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flash memory system of Application Note AP-678 or Application Note AP-629, each taken

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separately, particularly since the internal program verification operations are taught to be

redundant.

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy

as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS

from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of

the mailing date of this final action and the advisory action is not mailed until after the end of the

THREE-MONTH shortened statutory period, then the shortened statutory period will expire on

the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory

period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned

are as follows:

(703) 746-7238

(After Final Communications)

(703) 746-7239

(Official Communications)

<u>-</u>

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(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE ()
PRIMARY EXAMINER
ART UNIT 2187